

## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,570	01/14/2000	Gary L. Swoboda	TI-28933	8552
23494	7590 03/14/200	3		
TEXAS INSTRUMENTS INCORPORATED			EXAMINER	
P O BOX 65 DALLAS, T	5474, M/S 3999 X 75265		PHAN, THAI Q	
			ART UNIT	PAPER NUMBER
			2123	
			DATE MAILED: 03/14/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No. 09/483,570 Applicant(s)

Gary L. Swoboda

Examiner

Thai Phan

Art Unit 2123

Period for Reply  A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE MONTH(S) FROM  THE MAILING DATE OF THIS COMMUNICATION.  Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the	
THE MAILING DATE OF THIS COMMUNICATION.	
mailing date of this communication.	
If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Amy reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).	
Status	
1) Responsive to communication(s) filed on <u>Dec 20, 2002</u>	·
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.	
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11; 453 O.G. 213.	S
Disposition of Claims	
4) Claim(s) 1-4 is/are pending in the application	on.
4a) Of the above, claim(s) is/are withdrawn from consideration is a second consideration of the above, claim(s) is/are withdrawn from consideration is a second consideration of the above, claim(s) is	deration.
5) Claim(s) is/are allowed.	
6) 💢 Claim(s) 1-4 is/are rejected.	
7) Claim(s) is/are objected to.	
8) Claims are subject to restriction and/or election requ	uirement.
Application Papers	
9) The specification is objected to by the Examiner.	
10) ☐ The drawing(s) filed on is/are a) ☐ accepted or b) ☐ objected to by the Examiner.	
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).	
11) ☑ The proposed drawing correction filed on <u>Dec 20, 2002</u> is: a) ☑ approved b) ☐ disapproved by the	Examiner.
If approved, corrected drawings are required in reply to this Office action.	
12) The oath or declaration is objected to by the Examiner.	
Priority under 35 U.S.C. §§ 119 and 120	
13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).	
a) All b) Some* c) None of:	
1.   Certified copies of the priority documents have been received.	
2. Certified copies of the priority documents have been received in Application No.	
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).	
*See the attached detailed Office action for a list of the certified copies not received.	
14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).	
a) U The translation of the foreign language provisional application has been received.	
15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.	
Attachment(s)  1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413) Paper No(s)	
2) Notice of Dreftsperson's Patent Drawing Review (PTO-948)  5) Notice of Informal Patent Application (PTO-152)	
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	

Application/Control Number: 09/483,570

Art Unit: 2123

#### **DETAILED ACTION**

This Office Action is response to applicant's amendment filed on 12/20/2002. Claims 1-4 are pending in this Office Action.

# Specification

1. Due to applicant's amendment, the objection to the disclosure has been withdrawn.

## Drawings.

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 12/20/2002 have been approved.

#### Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al., US patent no. 6,075,941.

As per claim 1, Itoh discloses method of emulation of an integrated circuit including a CPU capable of executing program instruction with feature limitations substantially similar to the

Application/Control Number: 09/483,570

Art Unit: 2123

claimed invention (Abstract and Summary of the Invention). According to Itoh, the method includes steps of

detecting a predetermined debug event (col. 11, line 57 to col. 12, line 33, for example), upon detection of the predetermined debug event suspending program execution except for at least one type of interrupt (col. 16, line 23 to col. 18, line 23),

and executing the monitor program during program debugged via at least one type interrupt (cols. 17-19).

Itoh further discloses the emulator (ICE) (14) having control function for monitoring and controlling the operation of the CPU processor via debug interrupt (Summary and Background of the Invention). Itoh does not expressly disclose an emulation monitor program

Practitioner in the art at the time of the invention was made would have found Itoh ICE emulator program for monitoring and controlling the CPU processor operation as above could obviously imply emulation monitor program as claimed because the monitor program is executed and controlled in the emulator and for the emulator to monitor the operative state of the microcomputer.

5. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. as applied to claim 1 above, and further in view of Swoboda et al., US patent no. 6,522,985 B1.

As per claim 2, Itoh discloses selectively assigning emulation resources to one of emulation program to monitor signals for the ICE to detect the operating state of the microcomputer (col. 3, lines 20-54) through trace control circuit (34) for tracing control registers

and data buses or paths. Itoh does not expressly disclose serial scan path as claimed. Such feature is however well-known in the art. In fact, Swoboda teaches serial scan path for debugging and monitoring circuit emulation (Figs. 49, 50,, Abstract, Front page) to reduce emulation time and cost due to design change and grading as suggested in the Background of the invention.

This would motivate practitioner in the art at the time of the invention was made to combine Swoboda (US 6,522,985 B1) serial scan test into Itoh for emulation control of the logic circuit associated with the emulation system to reduce time and cost due to design change and grading as taught in Swoboda.

As per claim 3, Itoh discloses privilege input for monitor program, monitor of privilege input for the emulation program and assigning resources for emulation program and path tracing circuit. Swoboda teaches serial scan testability and emulation resource assignment to the circuit during circuit emulation as claimed.

As per claim 4, Itoh discloses emulation resources and accessing to the emulation resources through read/write data register (Figs. 3-20, col. 8, lines 26-59, cols. 9-13, for example).

### Response to Arguments

6. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Application/Control Number: 09/483,570 Page 5

Art Unit: 2123

#### Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- 1. US patent no. 6,370,606 B1, issued to Bonola, Thomas, on Apr. 2002
- 1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

## Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

# or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

Application/Control Number: 09/483,570

Art Unit: 2123

Page 6

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

March 9, 2003

Vrag Pateut Examiner 4V2123